REMARKS

Present Status of the Application

The Office Action rejected all presently pending claims 1-16. Specifically, claims 2 and 7-16 are rejected under 35 U.S.C. 112, second paragraph, claims 1, 4-5, 7 and 10-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Jang et al., claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al. in view of Sikora, and claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al. in view of Chua et al. In addition, clams 1, 3-5 and 9-10 are objected to because of some informalities.

Applicants have amended claims 1-5 and 7-10 to correct various informalities. No new matter adds through the amendments. Reconsideration of claims 1-16 is respectfully requested.

Rejections under 35 U.S.C. 112

With respect to claims 2 and 8, Applicants have amended them by specifying that the distance between neighboring "dense via holes is smaller than that between "isolated via holes". Thus, the relationship between "isolated via holes" and "denser via holes" is clear and definite. Support for this amendment can be found on page 7, second paragraph of the specification.

Claim 7 has been rewritten into independent form. Claims 8-16 are properly dependent upon claim 7.

Rejections under 35 U.S.C. 102(e)

Claims 1, 4-5, 7, 10-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Jang et al.

Applicant has amended claims 1 and 7. Independent claims 1 and 7 have at least one feature of "*performing an etching step to remove a portion of the gap fill polymer layer remaining in the via hole, in order to form a partial gap fill polymer while the dielectric layer is substantially not etched in this etching step*" that is not disclosed in the prior art. The feature is recited in claims 1 and 7 as follows, marked by underlines:

1. A dual damascene partial gap fill polymer fabrication process, comprising:

.....

covering the dielectric layer with a gap fill polymer, to fill the via hole;

performing a chemical mechanical polishing step to remove the gap fill polymer layer on the outside of the via hole;

performing an etching step to remove a portion of the gap fill polymer layer remaining on the inside of the via hole, forming a partial gap fill polymer, while the dielectric layer is substantially not etched in this etching step;

.....

7. A dual damascene partial gap fill polymer fabrication process, comprising:

.....

covering the second dielectric layer with a gap fill polymer layer, to fill the via hole;

performing a chemical mechanical polishing step to remove gap fill polymer layer on the outside of the via hole;

performing an etching step to remove a portion of the gap fill polymer layer remaining in the via hole, in order to form a partial gap fill polymer, while the dielectric layer is substantially not etched in this etching step;

.....

Jang et al. fail to teach or suggest the above emphasized feature. As illustrated in FIGs. 2-4 and described in col. 9, line 54-col. 10, line 26, and Col. 10, lines 53-58, the CMP planarization of the sacrificial via fill layer 24 is *immediately followed by the formation of a pair of second patterned photoresist layers 26a and 26b*. Then, with a second etching plasma 28, the sacrificial via fill layer 24 ***together with*** the patterned second dielectric layers 18a and 18b are etched. Therefore, the sacrificial via fill layer 24 is not etched into a ***partial*** via fill layer without substantially etching the surrounding dielectric layer. While in the present invention, as illustrated in FIG. 3D (362a/b) and described on page 7, lines 12-23 of the specification, the fill gap polymer 362 is etched to form the partial fill gap polymer 362a and 362b substantially without simultaneously etching the surrounding dielectric layer. The dielectric layer 350 is etched in a subsequent separate etching step.

For at least the reasons mentioned above, Applicants respectfully submit that independent claims 1 and 7 are not anticipated by, and patently define over Jang.

For at least the same reasons, Applicants respectfully submit that claims 4-5 and 10-15 dependent from claims 1 and 7, respectively, also patently define over Jang.

Rejections under 35 U.S.C. 103(a)

Claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al. in view of Sikora, and claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al. in view of Chua et al.

As mentioned above, Jang et al. fails to teach or suggest the above-mentioned feature of claims 1 and 7. Sikora also fails to teach or suggest the feature. Moreover, Chua et al. also fail to teach or suggest the feature. Therefore, Sikora and Chua cannot cure the deficiencies of jang and the features of claims 1 and 7 cannot be obtained by combining Jang et al. and Sikora (or Chua et al.). Therefore, claims 1 and 7 are patentable over Jang, Sikora, and Chua.

For at least the same reasons, claims 3, 6, 9 and 16 dependent from claims 1 and 7, respectively, patently define over the prior art.

CONCLUSION

For at least the foregoing reasons, it is believed that pending claims 1-16 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

Date: 3/28/2003

Jiawei Huang
Registration No. 43,330

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761

VERSION WITH MARKINGS TO SHOW WHERE CHANGES MADE

In The Claims

Please amend claims 1-5 and 7-10 as follows:

1. A dual damascene partial gap fill polymer fabrication process, comprising:

providing a substrate having a conductive layer therein;

forming a dielectric layer over the substrate and conductive layer;

forming at least one via hole in the dielectric layer, to expose a portion of the conductive layer;

covering the dielectric layer with a gap fill polymer, to fill the via hole;

performing a chemical mechanical polishing step to remove the gap fill polymer layer on the outside of the via hole;

performing an etching step to remove a portion of the gap fill polymer layer remaining on the inside of the via hole, forming a partial gap fill polymer, while the dielectric layer is substantially not etched in this etching step;

performing a lithographic process to form a photoresist layer having an opening above the dielectric layer, wherein the [trench] opening exposes the via hole and the partial gap fill polymer;

etching a portion of the dielectric layer exposed in the opening, to form a trench in the dielectric layer;

removing the photoresist layer and the partial gap fill polymer, to expose a portion of the conductive layer; and

filling the via hole and the trench with a metal material, to simultaneously form a plug and a first conductive line.

2. The method of claim 1, wherein forming at least one via hole includes forming [an] a plurality of isolated via holes and a plurality of dense via holes, wherein a distance between neighboring dense via holes is smaller than a distance between neighboring isolated via holes.

3. The method of claim 1, wherein the etching step for removing a portion of the gap fill polymer layer remaining on the inside of the via hole includes anisotropic etching.

4. The method of claim 1, wherein the [dielectric] conductive layer in the substrate includes

a second conductive line.

5. The method of claim 1, wherein a material of the dielectric layer [include] includes silicon oxide.

7. [The method of claim 1] A dual damascene partial gap fill polymer fabrication process, [further] comprising [the following steps]:

providing a substrate having a conductive layer therein, and a passivation layer formed over the conductive layer;

sequentially forming a first dielectric layer, a first etching stop layer and a second dielectric layer over the passivation layer;

sequentially patterning the second dielectric layer, the etching stop layer and the first dielectric layer to form at least one via hole, which exposes a portion of the passivation layer;

covering the second dielectric layer with a gap fill polymer layer, to fill the via hole;

performing a chemical mechanical polishing step to remove gap fill polymer layer on the outside of the via hole;

performing an etching step to remove a portion of the gap fill polymer layer remaining in the via hole, in order to form a partial gap fill polymer, while the second dielectric layer is substantially not etched in this etching step;

performing a lithographic process to form a photoresist layer having an opening above the second dielectric layer, wherein the [trench] opening exposes the via hole and the partial gap fill polymer;

etching [an exposed] the exposed second dielectric layer until the etching stop layer is reached, to form a trench in the second dielectric layer;

removing the photoresist layer and the partial gap fill polymer;

removing the passivation layer on a bottom of the via hole to expose a portion of the [dielectric] conductive layer; and

filling the trench with a metal material to simultaneously form a plug and a first conductive line.

8. The method of claim 7, wherein forming at least one via hole includes forming [an] a plurality of isolated via holes and a plurality of dense via holes, wherein a distance between

neighboring dense via holes is smaller than a distance between neighboring isolated via holes.

9. The method of claim 7, wherein the etching step for removing a portion of the gap fill polymer layer remaining in the via hole includes [an] anisotropic etching.

10. The method of claim 7, wherein the [dielectric] conductive layer in the substrate includes a second conductive line.